ABSTRACT

The present invention provides a semiconductor integrated circuit device with a diagnosis circuit, which may not engrave the delay of logic element in the normal operation. In a latch provided at the output of a memory or at the input of a logic stage, a signal selector is provided in the feedback loop of the latch. The selector is switched in correspondence with the operation mode, such that it transfers the feedback signal in the normal operation, while it inputs the test signal in the test mode, in order to prevent the delay from increasing in the signal selector on the main path in the normal operation.